3710 ACM

Advanced Digital Power Instrumentation Package

3710 ACM / Modicon Modbus

Serial Communications Protocol and Register Map

Version 1.3

POWER MEASUREMENT

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1 INTRODUCTION

The 3710 ACM performs Modbus communications by emulating the Modicon 984 Programmable Controller. This document describes the Modbus communications protocol employed by the 3710 ACM and how to pass information into and out of the 3710 ACM in a Modbus network.

This document provides the information necessary for a 3rd party OEM to develop in-house software to communicate with the 3710 ACM in a Modbus network.

Additional information concerning 3710 ACM operation can be found in the main chapters of the 3710 ACM Installation And Operation Manual.

1.1 PURPOSE OF THE COMMUNICATIONS PROTOCOL

The purpose of the 3710 ACM Modbus communications protocol is to allow setup information and measured data to be efficiently transferred between a Modbus Master Station and a 3710 ACM. This includes:

1) Allowing configuration and interrogation of all 3710 ACM set-up parameters from a Modbus Master Station.

2) Allowing interrogation of all data measured by a 3710 ACM, including minimum and maximum real time values and date stamps.

3) Allowing the configuration and interrogation of 3710 ACM setpoint parameters.

4) Allowing the control of the 3710 ACM relays.

5) Allowing the interrogation of the event log.

2 DETAILED DESCRIPTION OF THE 3710 ACM MODBUS PROTOCOL

2.1 3710 ACM MODBUS PROTOCOL GROUND RULES

The 3710 ACM is designed to function as a slave device on the RS-485 or RS-232C communication standards. The RS-485 medium allows for multiple devices on a single loop, whereas the RS-232C climate allows for only a single device. The 3710 ACM Modbus protocol is identical for both environments.

The following rules define the protocol for information transfer between a Modbus Master device and the 3710 ACM

1) All communications on the communications loop conforms to a MASTER/SLAVE scheme. In this scheme, information and data is transferred between a Modbus MASTER device and up to 32 SLAVE monitoring devices for RS-485 and only 1 SLAVE device for RS-232C.

2) The MASTER will initiate and control all information transfer on the communications loop.

3) Under no circumstances will a SLAVE device initiate a communications sequence.

4) All communications activity on the loop occurs in the form of "PACKETS", a packet being simply a serial string of 8-bit bytes. The maximum number of bytes contained within one packet is 255.

   The bytes that comprise a packet consist of standard asychronous serial data which are generated using equipment similar to that used for RS-232C.

2.2 MODES OF TRANSMISSION

Modbus protocol supports ASCII and RTU modes of transmissions. The 3710 ACM supports only the RTU mode of transmission with 8 data bits, no parity, and one stop bit.

2.3 DESCRIPTION OF THE MODBUS PACKET STRUCTURE

Every Modbus packet consists of four fields:

1) The Address Field
2) The Function Field
3) The Data Field
4) The Error Check Field (Checksum)

2.3.1 ADDRESS FIELD

The address field is 1-byte long and identifies which slave device the packet is for. Valid addresses range between 1 and 247. The slave device whose address matches the value in this field will perform the command specified in the packet.

2.3.2 FUNCTION FIELD

The function field is 1-byte long and tells the addressed slave which function to perform. The Modbus functions supported by the 3710 ACM are listed in Figure 2.1.

2.3.3 DATA FIELD

The Data Field varies in length depending on whether the message is a request or a response packet. This field typically contains information required by the slave device to perform the command specified in a request packet or data being passed back by the slave device in a response packet.

In general, data in this field are contained in either 16-bit or 32-bit registers. In 16-bit mode, registers are transmitted in the order of high-order byte first, low order byte second. In 32-bit mode, registers are transmitted in the order of high-order word first, low-order word second. For example, a 3710 ACM real-time parameter has the content 0012ABCD Hex,

In 16-bit mode, only the low-order register is transmitted:

High order byte = AB Hex
Low order byte = CD Hex

This register will be transmitted in the order AB CD.

In 32-bit mode, both the high-order and the low-order registers are transmitted:

High order word:
High order byte = 00 Hex
Low order byte = 12 Hex
Low order word:
High order byte = AB Hex
Low order byte = CD Hex

This register is transmitted in the order 00 12 AB CD.

FUNCTION	MEANING	ACTION
03	Read Holding Registers	Obtains the current value in one or more holding registers of the 3710 ACM.
16	Preset Multiple Registers	Places specific binary values into a series of consecutive holding registers of the 3710 ACM. The holding registers that can be written to a 3710 ACM are the time of day registers, the relay control registers, the setpoint parameter registers and the setup parameters.

Figure 2.1 Modbus Functions Supported by the 3710 ACM

2.3.4 ERROR CHECK FIELD (CHECKSUM)

This field allows the receiving device to determine if a packet has been corrupted with transmission errors. In Modbus RTU mode, the 16-bit Cyclic Redundancy Check (CRC-16) is used. The sending device calculates a 16-bit value, based on the information stored in the address, function and data fields using the CRC-16 algorithm and appends it to the end of the packet. The receiving device performs the same calculation upon the reception of a packet. If the result does not match the checksum stored in the packet, transmission errors have occurred and the packet will be ignored by the receiving device.

2.4 NETWORK TIMING CONSIDERATIONS

Network timing for the transfer of packets between units on the RS-485 loop must conform to the following rules:

1) The time between the end of a MASTER STATION message request packet and the beginning of a SLAVE STATION response packet is packet size dependent.

   T response time = [packet size dependent]

minimum	maximum	typical
20 ms	1000 ms	300 ms

2) The minimum time between the end of a SLAVE STATION response packet and the beginning of the next MASTER STATION message packet is device dependent.

   T slave min = [device dependent]

   Note that this is typically 100 milliseconds in 16-bit mode and can be as high as 1000 milliseconds in 32-bit mode for the 3710 ACM. This is true because *a maximum of 1 command packet per second is allowed in 32-bit mode*.

3) The maximum time between any two data bytes within a packet is baudrate dependent.

   T byte max = 3-byte time (3 milliseconds at 9600 baud, 6 milliseconds at 4800 baud, etc...).

   Note that this is typically less than 1 millisecond for the 3710 ACM.

4) When operating in RS-232C mode, the 3710 ACM controls the RTS line in the following manner. Immediately after receiving a valid Modbus request packet, the 3710 ACM asserts the RTS line. The response packet is then sent out after a minimum of 10ms have elapsed. The RTS line is held asserted throughout the transmission of the response packet and is de-asserted after transmission of the final CRC-16 checksum byte.

2.5 EXCEPTION RESPONSES

If a Modbus master device sends an invalid command to a 3710 ACM or attempts to read an invalid holding register, an exception response will be generated. The exception response consists of the slave address, function code, error code, and error check field. The high order bit of the function code is set to 1 to indicate that the packet is an exception response. Figure 2.2 describes the exception codes supported by the 3710 ACM and their possible causes.

CODE	NAME	MEANING
01	Illegal Function	An invalid command is contained in the function field of the request packet. The 3710 ACM only supports Modbus functions 3 and 16. This illegal function code could also mean that an incorrect password is used when the user attempts to perform a protected function.
02	Illegal Data Address	The address referenced in the data field is an invalid address for the specified function. This could also mean that the registers requested are not within valid register range of the 3710 ACM.

Figure 2.2 Exception Codes supported by the 3710 ACM

2.6 BROADCAST PACKETS

The 3710 ACM Modbus communications protocol supports the use of broadcast packets. The purpose of broadcast packet is to allow all Slave devices to receive the same command from the Master station. This feature is very useful in situations such as time synchronization of Slave clocks.

When broadcast packets are transmitted by the Master loop controller, all Slave devices will receive and perform the packet command, but must never send a response packet. This is to avoid the possibility of having more than one Slave device respond at one time.

The Preset Multiple Registers (Figure 2.1) command is the only command supporting broadcast packets. To send a broadcast packet, the destination Slave address must be set to 00 Hex.

3 PACKET COMMUNICATIONS

Two Modbus functions are supported by the 3710 ACM as illustrated in Figure 1.1. The standard Modbus protocol supports only 16-bit registers, which limit the maximum value of any measurement to 65535. To support applications which require large measurements, an extended 32-bit register mode is implemented in the 3710 ACM.

Section 3.1 discusses the differences between 16-bit and 32-bit communications. Section 3.2 discusses the Read Holding Registers packet of the 3710 ACM and its response packet. Section 3.3 discusses the Preset Multiple Registers packet and the acknowledge packet issued by the 3710 ACM.

3.1 16-BIT/32-BIT COMMUNICATIONS

In 16-bit mode, most parameters are passed in a single 16-bit register, and the maximum value is limited to 65535 even if the actual data exceeds 65535. In 32-bit mode, parameters are passed in the following manners:

1) Real-time and setup parameters except hour counters are passed in two distinct registers:

   High-Order register = $\frac{\text{value}}{10000}$

   Low-Order register = value **modulus** 10000.

   This configuration is compatible with the Modicon PLC floating point format.

2) For polarity registers, the high-order register always reads zero, and the low-order register contains the content of the polarity register.

3) Time stamps of the minimum and maximum data, as well as the event log are stored in a compressed 32-bit time format. In 16-bit mode, a value of 65535 will be returned for all time stamps.

	High-order register				Low-order register		
Bit #	31-30	29-26	25-21	20-16	15-10	09-04	03-00
	A	B	C	D	E	F	G

A) 2bits: Unused
B) 4 bits: Month (1-12)
C) 5 bits: Day (1-31)
D) 5 bits: Hour (0-23)
E) 6 bits: Minutes (0-59)
F) 6 bits: Seconds (0-59)
G) 4 bits: Year (1-10)

4) Hour counters (KWH, KVARH, KVAH) are always stored in two registers, whether 16-bit or 32-bit:

16-BIT MODE:

High-Order 16-bit = $\frac{\text{value}}{1000}$

Low-Order 16-bit = value **modulus** 1000.

32-BIT MODE:

High-Order 32-bit register:
High-Order 16-bit = 0.
Low-Order 16-bit = $\frac{\text{value}}{1000000}$

Low-Order 32-bit register:
High-Order 16-bit = $\frac{\text{value}}{10000}$ **modulus** 100.
Low-Order 16-bit = value **modulus** 10000.

The maximum value for hour counters is 65000 MWH in16-bit mode and 1000 GWH in 32-bit mode.

3.2 READ HOLDING REGISTERS (Function 03)

This command packet requests that the 3710 ACM respond with the number of registers specified beginning at the Start Address. Typically no password is required to read the registers. There is, however, one case where the correct password is required.

1) To read a protected register. Presently the only protected register is the register where the meter password is held.

Since there is no reserved password field in the Modbus protocol, a special procedure is required to read a protected register.

The password must first be written to the ***Packet Password*** register(address 43051) using the Preset Multiple Registers function(see Section 3.3). A response packet is always sent back regardless of the correctness of the password. The user may then perform the desired function. If the password previously transmitted is incorrect, an ***illegal function*** exception is generated; otherwise, the 3710 ACM will perform the specified command. Figure 3.1 illustrates the structure of the Read Holding Registers Packet.

16-BIT MODE

READ REGISTERS PACKET (Modicon 984 PC to 3710 ACM)	
Unit ID/Slave Address	(1 byte)
03 (Function Code)	(1 byte)
Start Address	(2 bytes)
# of Registers to Read	(2 bytes)
CRC Checksum	(2 bytes)
...	

READ REGISTERS RESPONSE PACKET (3710 ACM to Modicon 984 PC)	
Unit ID/Slave Address	(1 byte)
03 (Function Code)	(1 byte)
Byte Count (2 x # of registers)	(1 byte)
First Register in range	(2 bytes)
Second Register in range	(2 bytes)
...	
CRC Checksum	(2 bytes)

32-BIT MODE

READ REGISTERS PACKET (Modicon 984 PC to 3710 ACM)	
Unit ID/Slave Address	(1 byte)
03 (Function Code)	(1 byte)
Start Address	(2 bytes)
# of Registers to Read	(2 bytes)
CRC Checksum	(2 bytes)

READ REGISTERS RESPONSE PACKET (3710 ACM to Modicon 984 PC)	
Unit ID/Slave Address	(1 byte)
03 (Function Code)	(1 byte)
Byte Count (2 x # of registers)	(1 byte)
First Register H.O. word	(2 bytes)
First Register L.O. word	(2 bytes)
Second Register H.O. word	(2 bytes)
Second Register L.O. word	(2 bytes)
...	
CRC Checksum	(2 bytes)

NOTES

1) Only valid registers will be sent in a response packet. Registers which do not exist for a given voltage mode will not be sent. The user should ensure that the registers requested are available for a given voltage mode. For example, if the user attempts to read one register starting at address 40031 (KW Phase A), and the 3710 ACM is configured for DELTA voltage mode, the meter will return the contents of the first available register, 40034 (KW Total). No exception response will be generated.

2) In 32-bit mode, the number of registers to read should be twice that specified in 16-bit mode. For example, 20 registers are required to read 10 parameters in 32-bit mode, while only 10 registers are required to achieve the same result in 16-bit mode.

3) If the user requests more registers than there are available in the 3710 ACM, or if the registers requested are not within valid range of the 3710 ACM, an ***illegal address*** exception will be generated.

Figure 3.1 Read Holding Registers Packet

3.3 PRESET MULTIPLE REGISTERS (Function 16)

This command packet allows the Modbus master (Modicon PLC) to program the 3710 ACM. The registers that can be written to include the time clock, relay status registers, setpoint parameters, and 3710 ACM setup parameters. The meter's password is required in order to write to these registers. The procedure is identical to the Read Protected Register described in section 3.2.

16-BIT MODE

PRESET REGISTERS PACKET (Modicon 984 PC to 3710 ACM)		PRESET REGISTERS RESPONSE PACKET (3710 ACM to Modicon 984 PC)	
Unit ID/Slave Address	(1 byte)	Unit ID/Slave Address	(1 byte)
16 (Function Code)	(1 byte)	16 (Function Code)	(1 byte)
Start Address	(2 bytes)	Start Address	(2 bytes)
# of Registers to Write	(2 bytes)	# of Registers to Write	(2 bytes)
Byte Count (2 x # of registers)	(1 byte)	CRC Checksum	(2 bytes)
First Register	(2 bytes)		
Second Register	(2 bytes)		
...			
CRC Checksum	(2 bytes)		

32-BIT MODE

PRESET REGISTERS PACKET (Modicon 984 PC to 3710 ACM)		PRESET REGISTERS RESPONSE PACKET (3710 ACM to Modicon 984 PC)	
Unit ID/Slave Address	(1 byte)	Unit ID/Slave Address	(1 byte)
16 (Function Code)	(1 byte)	16 (Function Code)	(1 byte)
Start Address	(2 bytes)	Start Address	(2 bytes)
# of Registers to Write	(2 bytes)	# of Registers to Write	(2 bytes)
Byte Count (2 x # of registers)	(1 byte)	CRC Checksum	(2 bytes)
First Register H.O. Word	(2 bytes)		
First Register L.O. Word	(2 bytes)		
Second Register H.O. Word	(2 bytes)		
Second Register L.O. Word	(2 bytes)		
...			
CRC Checksum	(2 bytes)		

NOTES

1) The 3710 ACM assumes that the holding registers being written to are contiguous and in sequential order beginning at the Start Address.

2) In 32-bit mode, the number of registers to write should be twice that specified in 16-bit mode. For example, 20 registers are required to write 10 parameters in 32-bit mode, while only 10 registers are required to achieve the same result in 16-bit mode.

Figure 3.2 Preset Multiple Registers Packet

4 CALCULATING THE CRC-16 ERROR CHECK FIELD

4.1 PROCEDURE

This section describes the procedure for obtaining the CRC-16 error check field. A packet can be considered as a continuous, serial stream of binary data (ones and zeros). The 16-bit checksum is obtained by multiplying the serial data stream by 2^{16}(10000000000000000) and then dividing it by the ***generator polynomial*** $x^{16}+x^{15}+x^2+1$, which can be expressed as a binary data 11000000000000101. The quotient is ignored and the 16-bit remainder is the checksum and is appended to end of the packet. The receiving device performs the same operation on the entire packet including the checksum. The packet, when divided by the generator polynomial, should give a zero remainder if no transmission errors has occurred. In calculating the CRC, all arithmetic operations (additions and subtractions) are performed using MODULO TWO, or EXCLUSIVE OR operation. Figure 4.1 provides a step by step example to show how to obtain the checksum for a packet requesting one holding register at location 10 (Van of the 3710 ACM) from a slave with address 100 (64 Hex).

Steps for generating the CRC-16 checksum:

1) Form a new polynomial by dropping the MSB (Most Significant Bit) of the generator polynomial and reversing the bit sequence. This yields the binary number 1010 0000 0000 0001 or A0 01 Hex.
2) Load a 16-bit register with initial value FF FF Hex.
3) Exclusive OR the first data byte with the low-order byte of the 16-bit register, storing the result in the 16-bit register.
4) Shift the 16-bit register one bit to the right.

5a) If the bit shifted out to the right is one, Exclusive OR the 16-bit register with the new generator polynomial, with result stored in the16-bit register. Return to step 4.

5b) If the bit shifted out to the right is zero, return to step 4.

6) Repeat steps 4 and 5 until 8 shifts have been performed.
7) Exclusive OR the next data byte with the 16-bit register.
8) Repeat steps 4 through 7 until all bytes of the packet have been Exclusive ORed with the 16-bit register and shifted 8 times.
9) The content of the 16-bit register is the checksum and is appended to the end of the packet.

Example packet (in Hex):	Slave Address	Function	Start Address	# of registers to read	Checksum
	64	03	00 0A	00 01	to be calculated

Step	Byte	Bits Shifted	Action	16-Bit Register	Bit Shifted out
2			Initial Value	1111 1111 1111 1111	
	1		Load First Data Byte	0000 0000 0110 0100	
3			Exclusive OR	1111 1111 1001 1011	
4		1	Shift 1 bit to the Right	0111 1111 1100 1101	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1101 1111 1100 1100	
4		2	Shift 1 bit to the Right	0110 1111 1110 0110	0

Figure 4.1a Example - CRC-16 Generation

Step	Byte	Bits Shifted	Action	16-BIT REGISTER	Bit Shifted out
4		3	Shift 1 bit to the Right	0011 0111 1111 0011	0
4		4	Shift 1 bit to the Right	0001 1011 1111 1001	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1011 1011 1111 1000	
4		5	Shift 1 bit to the Right	0101 1101 1111 1100	0
4		6	Shift 1 bit to the Right	0010 1110 1111 1110	0
4		7	Shift 1 bit to the Right	0001 0111 0111 1111	0
4		8	Shift 1 bit to the Right	0000 1011 1011 1111	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1010 1011 1011 1110	
	2		Load Second Data Byte	0000 0000 0000 0011	
7			Exclusive OR	1010 1011 1011 1101	
4		1	Shift 1 bit to the Right	0101 0101 1101 1110	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1111 0101 1101 1111	
4		2	Shift 1 bit to the Right	0111 1010 1110 1111	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1101 1010 1110 1110	
4		3	Shift 1 bit to the Right	0110 1101 0111 0111	0
4		4	Shift 1 bit to the Right	0011 0110 1011 1011	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1001 0110 1011 1010	
4		5	Shift 1 bit to the Right	0100 1011 0101 1101	0
4		6	Shift 1 bit to the Right	0010 0101 1010 1110	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1000 0101 1010 1111	
4		7	Shift 1 bit to the Right	0100 0010 1101 0111	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1110 0010 1101 0110	
4		8	Shift 1 bit to the Right	0111 0001 0110 1011	0

Figure 4.1 (Continued)

Step	Byte	Bits Shifted	Action	16-BIT REGISTER	Bit Shifted out
	3		Load Third Data Byte	0000 0000 0000 0000	
7			Exclusive OR	0111 0001 0110 1011	
4		1	Shift 1 bit to the Right	0011 1000 1011 0101	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1001 1000 1011 0100	
4		2	Shift 1 bit to the Right	0100 1100 0101 1010	0
4		3	Shift 1 bit to the Right	0010 0110 0010 1101	0
4		4	Shift 1 bit to the Right	0001 0011 0001 0110	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1011 0011 0001 0111	
4		5	Shift 1 bit to the Right	0101 1001 1000 1011	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1111 1001 1000 1010	
4		6	Shift 1 bit to the Right	0111 1100 1100 0101	0
4		7	Shift 1 bit to the Right	0011 1110 0110 0010	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1001 1110 0110 0011	
4		8	Shift 1 bit to the Right	0100 1111 0011 0001	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1110 1111 0011 0000	
	4		Load Fourth Data Byte	0000 0000 0000 1010	
7			Exclusive OR	1110 1111 0011 1010	
4		1	Shift 1 bit to the Right	0111 0111 1001 1101	0
4		2	Shift 1 bit to the Right	0011 1011 1100 1110	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1001 1011 1100 1111	
4		3	Shift 1 bit to the Right	0100 1101 1110 0111	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1110 1101 1110 0110	
4		4	Shift 1 bit to the Right	0111 0110 1111 0011	0

Figure 4.1 (Continued)

Step	Byte	Bits Shifted	Action	16-BIT REGISTER	Bit Shifted out
4		5	Shift 1 bit to the Right	0011 1011 0111 1001	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1001 1011 0111 1000	
4		6	Shift 1 bit to the Right	0100 1101 1011 1100	0
4		7	Shift 1 bit to the Right	0010 0110 1101 1110	0
4		8	Shift 1 bit to the Right	0001 0011 0110 1111	0
	5		Load Fifth Data Byte	0000 0000 0000 0000	
7			Exclusive OR	0001 0011 0110 1111	
4	5	1	Shift 1 bit to the Right	0000 1001 1011 0111	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1010 1001 1011 0110	
4		2	Shift 1 bit to the Right	0101 0100 1101 1011	0
4		3	Shift 1 bit to the Right	0010 1010 0110 1101	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1000 1010 0110 1100	
4		4	Shift 1 bit to the Right	0100 0101 0011 0110	0
4		5	Shift 1 bit to the Right	0010 0010 1001 1011	0
4		6	Shift 1 bit to the Right	0001 0001 0100 1101	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1011 0001 0100 1100	
4		7	Shift 1 bit to the Right	0101 1000 1010 0110	0
4		8	Shift 1 bit to the Right	0010 1100 0101 0011	0
	6		Load Sixth Data Byte	0000 0000 0000 0001	
7			Exclusive OR	0010 1100 0101 0010	
4		1	Shift 1 bit to the Right	0001 0110 0010 1001	0
4		2	Shift 1 bit to the Right	0000 1011 0001 0100	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1010 1011 0001 0101	
4		3	Shift 1 bit to the Right	0101 0101 1000 1010	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1111 0101 1000 1011	

Figure 4.1 (Continued)

Step	Byte	Bits Shifted	Action	16-BIT REGISTER	Bit Shifted out
4		4	Shift 1 bit to the Right	0111 1010 1100 0101	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1101 1010 1100 0100	
4		5	Shift 1 bit to the Right	0110 1101 0110 0010	0
4		6	Shift 1 bit to the Right	0011 0110 1011 0001	0
4		7	Shift 1 bit to the Right	0001 1011 0101 1000	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1011 1011 0101 1001	
4		8	Shift 1 bit to the Right	0101 1101 1010 1100	1
			Generator Polynomial	1010 0000 0000 0001	
5a			Exclusive OR	1111 1101 1010 1101	
			Result	Hex FD Hex AD	

Figure 4.1 (Continued)

The packet completed with the CRC-16 checksum is as follows:

Slave Address	Function	Start Address	# of Registers to read	CRC checksum
64	03	00 0A	00 01	AD FD

4.2 PSEUDOCODE FOR CRC-16 GENERATION

For the users who are familiar with computer programming, the following is the pseudocode for calculating the 16-bit Cyclic Redundancy Check.

Initialize a 16-bit register to FFFF Hex
Initialize the generator polynomial to A001 Hex.

```
FOR n = 1 to # of bytes in packet
BEGIN
    XOR nth data byte with the 16-bit register
    FOR bits_shifted = 1 to 8
    BEGIN
        SHIFT 1 bit to the right
        IF (bit shifted out EQUAL 1)
            XOR generator polynomial with the 16-bit register and store result in the 16-bit register
    END
END
```

The resulting 16-bit register contains the CRC-16 checksum

5 3710 ACM REGISTER LIST

All 3710 ACM measured data and setup parameters are treated as HOLDING REGISTERS of the Modicon 984 PC having addresses 4xxxx when communicating in Modbus protocol. According to the MODBUS protocol, in response to a request for register 4xxxx of a particular slave device (3710), the MODBUS master reads register xxxx-1 from the slave (3710). For example, register 40011 corresponds to register 10.

The following sections will describe in detail the coded values stored for various registers. The registers will be discussed in the order they appear on the 3710 ACM MODBUS REGISTER MAP.

A complete map of all 3710 ACM MODBUS registers can be found in Appendix A.

5.1 STATUS REGISTERS

The status registers indicate the state of the 3710 Relays, the four status inputs (S1-S4) and the state of the various setpoints.

5.1.1 RELAY STATUS REGISTERS

The Relay Status Registers (40201-40203) indicate and control the status of the 3710 ACM control relays. A relay can be forced by writing a new status to the associated status register.

Bit #	15-7	6	5	4	3	2	1	0
						B	A	

	READING	WRITING
A)	00 = Released	00=Normal
	01 = Operated	01=Force Operate
	10 = Forced Released	10=Force Release
	11 = Forced Operated	

B) 0 = Relay is latched
1 = Relay is pulsed

5.1.2 STATUS INPUT REGISTER

The Status Input Register (40210) indicates the status of the 3710 ACM Status Inputs (S1-S4).

Bit # 15-7 6 5 4 3 2 1 0

				B	C	D	E

B) Status Input #4: 0 = Normal, 1 = Active
C) Status Input #3: 0 = Normal, 1 = Active
D) Status Input #2: 0 = Normal, 1 = Active
E) Status Input #1: 0 = Normal, 1 = Active

5.1.3 SETPOINT STATUS REGISTERS

Setpoint Status Registers (40211 - 40227) indicate the setpoint key code of each setpoint, and whether the setpoint is currently active.

Bit #	15-8	7	6-5	4	3	2	1	0
		F	G					

F) Setpoint Status: 0 = Normal, 1 = Active
G) Setpoint Parameter - Setpoint index (0-127)

00	Not Used
01	Over Voltage
02	Under Voltage
03	Voltage Unbalance
04	Over Amperage
05	Amperage Unbalance
06	Over KVA
07	Over KW Forward
08	Over KW Reverse
09	Over KVAR Forward
10	Over KW Demand
11	Over Amp Demand
12	Over Frequency (x10)
13	Under Frequency (x10)
14	Over Vaux
15	Under Vaux
16	Phase Reversal
17	Under PF Lagging
18	Under PF Leading
19	Over I4
20	Over KVAR Reverse
21	S1 Input Normal
22	S1 Input Active
23	S2 Input Normal
24	S2 Input Active
25	S3 Input Normal
26	S3 Input Active
27	S4 Input Normal
28	S4 Input Active
29	SX Input Normal
30	SX Input Active

APPENDIX A

3710 ACM MODBUS REGISTER MAP

Note that, according to the MODBUS protocol, in response to a request for address 4xxxx, the master reads register xxxx-1 from the slave (3710). For example, a request for register 40011 returns register 10 from the slave.

Register Address	Reg. Type	Description	Notes
REAL TIME PARAMETERS			
40002	RW	Year (minus 1900)	
40003	RW	Month (1-12)	
40004	RW	Day (1-31)	
40005	RW	Hour (0-23)	
40006	RW	Minute (0-59)	
40007	RW	Second (0-59)	
40011	RO	Van	(a)
40012	RO	Vbn	(a)
40013	RO	Vcn	(a,b)
40014	RO	Vln average	(a)
40015	RO	Vab	
40016	RO	Vbc	(b)
40017	RO	Vca	(b)
40018	RO	Vaverage(l-l)	(c)
40020	RO	Vaux	
40021	RO	Ia	
40022	RO	Ib	
40023	RO	Ic	(b)
40024	RO	Iaver	
40026	RO	I4 Neutral Current	
40031	RO	KW Phase A	(a)
40032	RO	KW Phase B	(a)
40033	RO	KW Phase C	(a,b)
40034	RO	KW TOTAL	
40035	RO	KVAR Phase A	(a)
40036	RO	KVAR Phase B	(a)
40037	RO	KVAR Phase C	(a,b)
40038	RO	KVAR Total	
40042	RO	Power Factor	
40043	RO	KVA Phase A	(a)
40044	RO	KVA Phase B	(a)
40045	RO	KVA Phase C	(a,b)
40046	RO	KVA Total	
40048	RO	Freq on V1	
40050	RO	Real time polarity	(e)
40051	RO	KWH Import	
40052	RO	M/GWH Import	(d)
40053	RO	KWH Export	
40054	RO	M/GWH Export	(d)
40055	RO	KWH Total	
40056	RO	M/GWH Total	(d)
40061	RO	KVARH Import	
40062	RO	M/GVARH Import	(d)
40063	RO	KVARH Export	
40064	RO	M/GVARH Export	(d)
40065	RO	KVARH Total	
40066	RO	M/GVARH Total	(d)
40071	RO	KVAH	
40072	RO	M/GVAH	(d)
40081	RO	Iaver Demand or KVA Demand	(OPT)
40082	RO	KW Total Demand	
STATUS REGISTERS			
40201	RW	Relay #1	
40202	RW	Relay #2	
40203	RW	Relay #3	
40210	RO	Status Input	
40211	RO	Setpoint #01	
40212	RO	Setpoint #02	
40213	RO	Setpoint #03	
40214	RO	Setpoint #04	
40215	RO	Setpoint #05	
40216	RO	Setpoint #06	
40217	RO	Setpoint #07	
40218	RO	Setpoint #08	
40219	RO	Setpoint #09	
40220	RO	Setpoint #10	
40221	RO	Setpoint #11	

40222	RO	Setpoint #12	
40223	RO	Setpoint #13	
40224	RO	Setpoint #14	

Register Address	Reg. Type	Description	Notes
40225	RO	Setpoint #15	
40226	RO	Setpoint #16	
40227	RO	Setpoint #17	
40241	RO	S1 Input Counter	

MINIMUM REAL TIME VALUES

40311	RO	Van	(a)
40312	RO	Vbn	(a)
40313	RO	Vcn	(a,b)
40314	RO	Vln average	(a)
40315	RO	Vab	
40316	RO	Vbc	(b)
40317	RO	Vca	(b)
40318	RO	Vaverage (l-l)	(c)
40320	RO	Vaux	
40321	RO	Ia	
40322	RO	Ib	
40323	RO	Ic	(b)
40324	RO	Iaver	
40326	RO	I4 Neutral	
40334	RO	KW total	
40338	RO	KVAR total	
40342	RO	PF total	
40346	RO	KVA total	
40348	RO	Frequency	
40350	RO	Min real polarity	(e)
40381	RO	Iaver Dmd	
40382	RO	KW total Dmd	

MINIMUM TIME STAMPS (*)

40411	RO	Van	(a)
40412	RO	Vbn	(a)
40413	RO	Vcn	(a,b)
40414	RO	Vln average	(a)
40415	RO	Vab	
40416	RO	Vbc	(b)
40417	RO	Vca	(b)
40418	RO	Vaverage (l-l)	(c)
40420	RO	Vaux	

Register Address	Reg. Type	Description	Notes
40421	RO	Ia	
40422	RO	Ib	
40423	RO	Ic	(b)
40424	RO	Iaver	
40426	RO	I4 Neutral Current	
40434	RO	KW total	
40438	RO	KVAR total	
40442	RO	PF total	
40446	RO	KVA total	
40448	RO	Frequency	
40481	RO	Iaver Demand or KVA Demand	(OPT)
40482	RO	KW total Demand	

MAXIMUM REAL TIME VALUES

40611	RO	Van	(a)
40612	RO	Vbn	(a)
40613	RO	Vcn	(a,b)
40614	RO	Vln average	(a)
40615	RO	Vab	
40616	RO	Vbc	(b)
40617	RO	Vca	(b)
40618	RO	Vaverage (l-l)	(c)
40620	RO	Vaux	
40621	RO	Ia	
40622	RO	Ib	
40623	RO	Ic	(b)
40624	RO	Iaver	
40626	RO	I4 Neutral	
40634	RO	KW total	
40638	RO	KVAR total	
40642	RO	PF total	
40646	RO	KVA total	
40648	RO	Frequency	
40650	RO	Max real polarity	(e)
40681	RO	Iaver Demand	

		or KVA Demand	(OPT)
40682	RO	KW total Dmd	

Register Address	Reg. Type	Description	Notes
MAXIMUM TIME STAMPS (*)			
40711	RO	Van	(a)
40712	RO	Vbn	(a)
40713	RO	Vcn	(a,b)
40714	RO	Vln average	(a)
40715	RO	Vab	
40716	RO	Vbc	(b)
40717	RO	Vca	(b)
40718	RO	Vaverage (l-l)	(c)
40720	RO	Vaux	
40721	RO	Ia	
40722	RO	Ib	
40723	RO	Ic	(b)
40724	RO	Iaver	
40725	RO	I4 Neutral	
40734	RO	KW total	
40738	RO	KVAR total	
40742	RO	PF total	
40746	RO	KVA total	
40748	RO	Frequency	
40781	RO	Iaver Dmd	
40782	RO	KW total Dmd	

Register Address	Reg. Type	Description	Notes

SETPOINTS

General Setpoint Format		
+0	RW	Low limit
+1	RW	High Limit
+2	RW	Release time delay
+3	RW	Operate time delay
+4	RW	Relay number
+5	RW	Setpoint key

40902 - 40907	Setpoint #1
40912 - 40917	Setpoint #2
40922 - 40927	Setpoint #3
40932 - 40937	Setpoint #4
40942 - 40947	Setpoint #5
40952 - 40957	Setpoint #6
40962 - 40967	Setpoint #7
40972 - 40977	Setpoint #8
40982 - 40987	Setpoint #9
40992 - 40997	Setpoint #10
41002 - 41007	Setpoint #11
41012 - 41017	Setpoint #12
41022 - 41027	Setpoint #13
41032 - 41037	Setpoint #14
41042 - 41047	Setpoint #15
41052 - 41057	Setpoint #16
41062 - 41067	Setpoint #17

WAVEFORM CAPTURE (**)

41201	RO	Waveform channel #
41202	RO	# of sample points
41203	RO	Sample point delay (uS)
41204-41299	RO	128 Sample points
41204-41227	RO	32 Sample points

NOTES

** Waveform capture is a BLOCK READ command. To obtain the captured waveform, the following request must be sent:

If standard frequency has been set to 50 or 60 Hz:
Read 99 holding registers, starting at register 41201.
If the standard frequency has been set to 400 Hz:
Read 27 holding registers, starting at register 41201.

EVENT LOG

Register Address	Reg. Type	Description	Notes
General Event Format			
+0	RO	Event time	(*)
+1	RO	Year of event (minus 1900)	
+2	RO	Event flag	
+3	RO	Event code	
+4	RO	Event log value	
41501 - 41505		Event #1	(Most recent)
41506 - 41510		Event #2	
41511 - 41515		Event #3	
41516 - 41520		Event #4	
41521 - 41525		Event #5	
41526 - 41530		Event #6	
41531 - 41535		Event #7	
41536 - 41540		Event #8	
41541 - 41545		Event #9	
41546 - 41550		Event #10	
41551 - 41555		Event #11	
41556 - 41560		Event #12	
41561 - 41565		Event #13	
41566 - 41570		Event #14	
41571 - 41575		Event #15	
41576 - 41580		Event #16	
41581 - 41585		Event #17	
41586 - 41590		Event #18	
41591 - 41595		Event #19	
41596 - 41600		Event #20	
41601 - 41605		Event #21	
41606 - 41610		Event #22	
41611 - 41615		Event #23	
41616 - 41620		Event #24	
41621 - 41625		Event #25	
41626 - 41630		Event #26	
41631 - 41635		Event #27	
41636 - 41640		Event #28	
41641 - 41645		Event #29	
41646 - 41650		Event #30	
41651 - 41655		Event #31	
41656 - 41660		Event #32	
41661 - 41665		Event #33	
41666 - 41670		Event #34	
41671 - 41675		Event #35	
41676 - 41680		Event #36	
41681 - 41685		Event #37	
41686 - 41690		Event #38	
41691 - 41695		Event #39	
41696 - 41700		Event #40	
41701 - 41705		Event #41	
41706 - 41710		Event #42	
41711 - 41715		Event #43	
41716 - 41720		Event #44	
41721 - 41725		Event #45	
41726 - 41730		Event #46	
41731 - 41735		Event #47	
41736 - 41740		Event #48	
41741 - 41745		Event #49	
41746 - 41750		Event #50	(Least recent)

3710 ACM SETUP REGISTERS (MODBUS)

Register Address	Reg. Type	Description	Notes
43002	RW	Voltage Scale	
43003	RW	Vaux Scale	
43004	RW	Current Scale	
43005	RW	Volt. input mode	
43006	RW	Unit ID number	
43007	RW	Baud rate	
43008	RW	Demand period	
43009	RW	I4 Neutral scale	
43010	WO	Password	
43011	WO	Reset min/max	
43012	WO	Reset hour counters	
43013	RO	Firmware rev. numb.	
43015	RO	Feat. code	
43016	RO	Device type	
43018	RW	# of demand periods	
43021	RW	Phase sequence	
43022	RW	Iout range	
43023	RW	Iout key	
43024	RW	Iout Scale	
43025	RW	Standard Frequency	
43026	RO	Serial Comm. mode	
43027	RW	Relay #1 Mode	
43028	RW	Relay #1 Value	
43029	RW	Relay #2 Mode	
43030	RW	Relay #2 Value	
43031	RW	Relay #3 Mode	
43032	RW	Relay #3 Value	
43033	RW	Log status changes	
43034	RW	Waveform channel #	
43035	WO	Reset status #1 channel	
43051	WO	Packet password	(f)

NOTES

Register types: RO = Read Only
WO = Write Only
RW = Read/Write

* Time stamps are returned in a 32 bit compressed format. To access the time stamps, the meter must be set to 32 bit register size. If the register size is set to 16 bits, a value of 65535 will be returned.

OPT KVA Demand is an optional feature.

a. Not available in DELTA mode.

b. Not available in SINGLE PHASE mode.

c. Available in DELTA mode only.

d. Register size dependent: 16 BIT = MWH/MVARH/MVAH
32 BIT = GWH/GVARH/GVAH

e. Each bit in a polarity register indicates the polarity of a data register.
0 = Positive 1 = Negative

	POLARITY REGISTERS			
	Realtime	**Minimum**	**Maximum**	
BIT	**40050**	**40350**	**40650**	
0	40031	not used	not used	
1	40032	not used	not used	**D**
2	40033	not used	not used	**A**
3	40034	40334	40634	**T**
4	40035	not used	not used	**A**
5	40036	not used	not used	
6	40037	not used	not used	**R**
7	40038	40338	40638	**E**
8	40042	40342	40642	**G**
9	40081	40381	40681	**I**
10	40082	40382	40682	**S**
11	RESERVED FOR FUTURE USE			**T**
12	RESERVED FOR FUTURE USE			**E**
13	RESERVED FOR FUTURE USE			**R**
14	40055, 40056	not used	not used	**S**
15	40065, 40066	not used	not used	

f. A valid password must be written in the packet password register before one can write to other registers.

31	
...	RESERVED
127	

5.2 SETPOINTS REGISTERS

Registers 40902 - 41067 control the 3710 ACM setpoints. Each setpoint has six associated registers specifying the Low Limit, High Limit, Release Delay and Operate Delay times, as well as the Relay number and Setpoint Key.

5.2.1 SETPOINT KEY CODES

The Setpoint Key registers for each setpoint specifies the parameter that the setpoint will monitor, as specified by the following list:

00	NOT USED
01	OVER VOLTAGE
02	UNDER VOLTAGE
03	VOLTAGE UNBALANCE
04	OVER CURRENT
05	CURRENT UNBALANCE
06	OVER KVA
07	OVER KW FORWARD
08	OVER KW REVERSE
09	OVER KVAR FORWARD
10	OVER KW DEMAND
11	OVER AMP DEMAND
12	OVER FREQUENCY (x10)
13	UNDER FREQUENCY (x10)
14	OVER VAUX
15	UNDER VAUX
16	PHASE REVERSAL
17	UNDER PF LAGGING
18	UNDER PF LEADING
19	OVER I4
20	OVER KVAR REVERSE
21	S1 INPUT NORMAL
22	S1 INPUT ACTIVE
23	S2 INPUT NORMAL
24	S2 INPUT ACTIVE
25	S3 INPUT NORMAL
26	S3 INPUT ACTIVE
27	S4 INPUT NORMAL
28	S4 INPUT ACTIVE
29	SX INPUT NORMAL
30	SX INPUT ACTIVE

5.3 EVENT LOG

This log records events such as power up, parameter changes, alarm conditions, relay changes, and status input changes. The 50 most recent events are available through a total of 250 registers (5 register associated with each event). See the 3710 ACM MODBUS REGISTER MAP for a complete list of all Event Log Registers.

5.3.1 EVENT FLAG REGISTERS

The Event Flag Register for each event indicates the status of the 3710 ACM relays after the event occurred. In addition, the register specifies the relay that was operated or released when the setpoint became active.

Bit #	15-8	7	6	5	4-3	2	1	0
		A	B	C	D	E		F

A) Relay Status #3: 0 = Released, 1 = Operated
B) Relay Status #2: 0 = Released, 1 = Operated
C) Relay Status #1: 0 = Released, 1 = Operated
D) Relay Number: 00 = Relay #0
01 = Relay #1
10 = Relay #2
11 = Relay #3
E) Setpoint Status: 0 = Normal, 1 = Active
F) General Information 00 = No Data
01 = Front Panel Event
10 = Comm Packet Event
11 = Forced Relay Operation

5.3.2 EVENT CODES

The Event Code Register of each event indicates which type of event occurred, according to the following list:

000	Reserved
001	Setpoint Over Voltage
002	Setpoint Under Voltage
003	Setpoint Voltage Unbalance
004	Setpoint Over Amperage
005	Setpoint Amperage Unbalance
006	Setpoint Over KVA
007	Setpoint Over KW Forward
008	Setpoint Over KW Reverse
009	Setpoint Over KVAR Forward
010	Setpoint Over KW Demand
011	Setpoint Over Amp Demand

012	Setpoint Over Frequency (x10)
013	Setpoint Under Frequency (x10)
014	Setpoint Over Vaux
015	Setpoint Under Vaux
016	Setpoint Phase Reversal
017	Setpoint Under PF Lagging
018	Setpoint Under PF Leading
019	Setpoint Over I4
020	Setpoint Over KVAR Reverse
021	Setpoint S1 Input Normal
022	Setpoint S1 Input Active
023	Setpoint S2 Input Normal
024	Setpoint S2 Input Active
025	Setpoint S3 Input Normal
026	Setpoint S3 Input Active
027	Setpoint S4 Input Normal
028	Setpoint S4 Input Active
029	Setpoint SX Input Normal
030	Setpoint SX Input Active
031	Reserved for future expansion
032	Setpoint Over Voltage Phase A
033	Setpoint Over Voltage Phase B
034	Setpoint Over Voltage Phase C
035	Unused
036	Setpoint Under Voltage Phase A
037	Setpoint Under Voltage Phase B
038	Setpoint Under Voltage Phase C
039	Unused
040	Setpoint Voltage Unbalance Phase A
041	Setpoint Voltage Unbalance Phase B
042	Setpoint Voltage Unbalance Phase C
043	Unused
044	Setpoint Over Amperage Phase A
045	Setpoint Over Amperage Phase B
046	Setpoint Over Amperage Phase C
047	Unused
048	Setpoint Amps Unbalance Phase A
049	Setpoint Amps Unbalance Phase B
050	Setpoint Amps Unbalance Phase C
...	Unused
257	Time Set
258	Setup Changed
259	Alarms Changed
260	Power Up/Reset
261	Relay Control
262	Cleared Max/Min
263	Cleared Hours
...	Unused
268	Factory Clear
269	Firmware Revision
270	NV Failure
271	Frequency Failure
272	Hydro Failure
273	Setpoint Failure
274	Front Panel Failure
275	Propack Failure
276	ISR Failure
277	Init Failure
278	Calc Failure
279	Timer Failure
280	Status Input Failure
281	Status Input #1 - Normal
282	Status Input #2 - Normal
283	Status Input #3 - Normal
284	Status Input #4 - Normal
285	Status Input #1 - Active
286	Status Input #2 - Active
287	Status Input #3 - Active
288	Status Input #4 - Active
...	Unused
8191	

5.4 SETUP REGISTERS

The Setup Registers (43002-43035) provide a means to program the 3710 ACM from a remote location. The following sections discuss the setup registers which contain an encoded value.

5.4.1 VOLTAGE INPUT MODE

The Voltage Input Mode Register (43005) controls the operating mode of the 3710 ACM. The following modes are supported:

0	4-wire Wye
1	Delta
2	Single Phase
3	Demonstration
4	3-wire Wye

5.4.2 BAUD RATE

The Baud Rate Register (43007) controls the communications data rate for both RS-232C and RS-485 communications modes. The following baud rates are supported by the 3710 ACM:

300,1200,2400,4800,9600,19200

The baud rate can be selected by writing the above values to the Baud Rate Register.

5.4.3 RESET HOUR COUNTERS

The 3710 ACM hour counters (KWH, KVARH) can be reset by writing to the Reset Hour Counters register (43012). The following values can be written:

0	Counters are not reset.
1	Reset KWH counter.
2	Reset KVARH counter.
4	Reset KVAH counter.
7	Reset KWH, KVARH, and KVAH

5.4.4 PHASE SEQUENCE

The phase rotation sequence used for PF polarity detection in DELTA mode, and for the phase reversal detection setpoint is controlled by the Phase Sequence Register (43021).

0	ABC, XYZ, RYB, RST
1	ACB, XZY, RBY, RTS

5.4.5 I OUT RANGE

The I Out Range Registers (43022) indicates 0 to 20 mA or 4 to 20 mA proportional current output.

0	0-20 mA
1	4-20 mA

5.4.6 I OUT KEY CODES

The I Out Key Register (43023) specifies with which measured parameter the current output will be proportional.

00	Voltage Phase A
01	Voltage Phase B
02	Voltage Phase C
03	Current Phase A
04	Current Phase B
05	Current Phase C
06	KW Phase A
07	KW Phase B
08	KW Phase C
09	KVA Phase A
10	KVA Phase B
11	KVA Phase C
12	KVAR Phase A
13	KVAR Phase B
14	KVAR Phase C
15	Voltage Average
16	Current Average
17	KW Total
18	KVA Total
19	KVAR Total
20	Power Factor
21	KW Demand
22	AMP Demand
23	Frequency
24	VAUX
25	Neutral Current (I4)

5.4.7 SERIAL COMMUNICATIONS MODE

The Serial Communications Register is a READ ONLY register specifying the communications mode selected by the jumper on the 3710 Communications Card.

Bit #	15-7	6	5	4	3	2	1	0
								A

A) Serial Communications Mode 0 = RS-232
1 = RS-485

5.4.8 RELAY OPERATION MODE

The Relay Operation Mode Registers (43027-43032) control the operation of the 3710 ACM relays. Each relay can be assigned one of the following operation modes:

0	Setpoint
1	KWH Pulse (interval controlled by Relay Value register)
2	KVARH Pulse (interval controlled by Relay Value register)
3	KVAH Pulse (interval controlled by Relay Value register)

5.4.9 LOG STATUS CHANGES

The Log Status Changes Register (43033) specifies whether changes to the status inputs (S1-S4) are logged in the Event Log.

Bit #	15-12	11-8	7-4	3-0
	A	B	C	D

A) Log S4 status changes: 0=No, 1=Yes
B) Log S3 status changes: 0=No, 1=Yes

C) Log S2 status changes: 0=No, 1=Yes
D) Log S1 status changes: 0=No, 1=Yes

5.4.10 WAVEFORM CHANNEL

Before each waveform capture request, the desired channel must be written to the Waveform Channel register.

Channel #	Input (Wye)	Input (Delta)
0	V1-neutral	V1-2
1	I1	I1
2	V2-neutral	N/A
3	I2	I2
4	V3-neutral	V3-1
5	I3	I3
6	I4	I4
7	Vaux	Vaux

6 WAVEFORM CAPTURE

The 3710 ACM waveform capture feature allows signals at each of its voltage (V1, V2, V3, Vaux) inputs and current (I1, I2, I3, I4) inputs to be digitally sampled.

6.1 WAVEFORM READ REQUEST

Waveform Capture is a BLOCK READ command. To initiate and obtain a waveform capture, a Read Holding Registers packet with a preset starting address and a preset number of registers must be transmitted. See figure 6.1

Waveform samples will be returned in a compressed packet format. This format does not allow a Programmable Logic Controller to examine the data. However, PCs connected to the Modbus Plus network using Modicon interface products will be able to decode the compressed samples.

6.2 COMPRESSED SAMPLE FORMAT

The waveform samples are arranged in a packed format. In this format, two 12-bit samples are contained in three bytes (24-bits).

Data is in unsigned 12-bit format with two samples in every three-byte word. The three-byte word is ordered in the packet as low byte first, middle byte next and high byte last. The three-byte words are organised as follows:

Bit #	23-16	15-12	11-08	07-00
	A	B	C	D

A) Upper 8 bits of the first sample
B) Lower 4 bits of the first sample
C) Upper 4 bits of the second sample
D) Lower 8 bits of the second sample

The three-byte words continue in the same manner till the end of packet.

16/32-BIT MODE

WAVEFORM CAPTURE PACKET (Modicon 984 PC to 3710 ACM)		WAVEFORM CAPTURE RESPONSE (3710 ACM to Modicon 984 PC)	
Unit ID/Slave Address	(1 byte)	Unit ID/Slave Address	(1 byte)
03 (Function Code)	(1 byte)	03 (Function Code)	(1 byte)
1200 (Start Address)	(2 bytes)	54 or 198 (Byte Count)	(1 byte)
27 or 99 (# of Registers)	(2 bytes)	Waveform Channel #	(2 bytes)
CRC Checksum	(2 bytes)	Number of Sample Points	(2 bytes)
		Delay between each sample in microseconds	(2 bytes)
	...	Compressed Samples	(48/192 bytes)
		CRC Checksum	(2 bytes)

NOTES

1) The number of register requested depends on the Standard Frequency (register 43025) selected. If the 3710 ACM is configured for 50 or 60 Hz operation, 99 registers are requested. A total of 128 waveform samples will be returned in 192 compressed sample bytes. If configured for 400 Hz operation, 27 registers are requested. A total of 32 waveform samples will be returned in 48 compressed sample bytes.

2) The Waveform Capture Packet format is identical in both 16 and 32 bit register size modes.

3) If the user requests a waveform register without following the above BLOCK READ format, an ***illegal address*** exception will be generated.

Figure 6.1 Waveform Capture Packet

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